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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,987	11/30/2001	Feng Dai	CS00-197/199	3473

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GEORGE O. SAILE & ASSOCIATES
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER
PERKINS, PAMELA E

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,987	DAI ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- Th MAILING DATE of this communication appears on th cover sh t with the corresp nd nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This office action is in response to the filing of the application on 30 November 2001. Claims 1-25 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 3, 5, 6, 16, 18, 20 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (6,197,691)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Lee discloses a method of forming shallow trench isolation regions where a silicon nitride etch stop layer (34) in deposited using a chemical vapor process (CVD) on to a semiconductor substrate (30); etching a plurality of isolation trenches (Fig. 6) through the silicon nitride etch stop layer (34) into the semiconductor substrate (30), whereby narrow active areas and wide active areas of the semiconductor substrate (30) are left between the isolation trenches; depositing an oxide layer (38) over the silicon nitride etch stop layer (34) and within the isolation trenches using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (38) overlying the silicon nitride etch stop layer (34) and then removing the silicon nitride etch stop layer (34). Lee further discloses the silicon nitride etch stop layer (34) having a thickness between 1500 and 2500 Angstroms, and the removing the silicon nitride etch stop layer (34) with a hot phosphoric acid (H_3PO_4) dip (col. 3, lines 38-65; col. 4, lines 59-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4, 7, 8-10, 13-15, 17, 19 and 22-25 are rejected under 35 U.S.C. 103(a) as being obvious over Lee in view of Hao et al. (6,403,483).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Lee discloses a method of forming shallow trench isolation regions where a silicon nitride etch stop layer (34) in deposited using a chemical vapor process (CVD) on to a semiconductor substrate (30); etching a plurality of isolation trenches (Fig. 6) through the silicon nitride etch stop layer (34) into the semiconductor substrate (30),

whereby narrow active areas and wide active areas of the semiconductor substrate (30) are left between the isolation trenches; depositing an oxide layer (38) over the silicon nitride etch stop layer (34) and within the isolation trenches using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (38) overlying the silicon nitride etch stop layer (34) and then removing the silicon nitride etch stop layer (34). Lee further discloses the silicon nitride etch stop layer (34) having a thickness between 1500 and 2500 Angstroms, and the removing the silicon nitride etch stop layer (34) with a hot phosphoric acid (H_3PO_4) dip (col. 3, lines 38-65; col. 4, lines 59-65).

Referring to claims 18 and 23, Lee further discloses depositing a second silicon nitride etch stop layer (46), with a thickness between 250 and 750 Angstroms, over the oxide layer (38), removing the second silicon nitride etch stop layer (38) overlying the wide active areas, etching away the oxide layer (38) overlying the silicon nitride etch stop layer (34) and the removing the silicon nitride etch stop layer (34) and the second silicon nitride etch stop layer (46) (col. 4, lines 33-65). Lee does not disclose forming an oxide on the substrate prior to depositing the silicon nitride layer, lining the isolation trenches prior to depositing the oxide layer nor fabricating semiconductor device structures on the semiconductor substrate between the isolation trenches.

Hao et al. disclose a method of forming shallow trench isolation regions where an oxide layer (120) is formed on a semiconductor substrate (100), forming a silicon nitride etch stop layer (160) over the oxide layer (120), using a chemical vapor process (CVD); etching an isolation trench (220) through the silicon nitride etch stop layer (160) and the oxide layer (120) into the semiconductor substrate (100); lining the isolation trench with

an oxide (300); depositing an oxide layer (400) over the silicon nitride etch stop layer (160) and within the isolation trench (220) using a high density plasma (HDP); etching away the oxide layer (400) overlying the silicon nitride etch stop layer (160), then removing the silicon nitride etch stop layer (160) and further fabricating semiconductor device structures (710, 730) on the semiconductor substrate (100) between the isolation trench (220). Hao et al. further disclose the silicon nitride etch stop layer (160) having a thickness between 2000 and 4000 Angstroms (col. 3, lines 1-51).

Since Lee and Hao et al. are both from the same field of endeavor, a method of forming shallow trench isolation regions, the purpose disclosed by Hao et al. would have been recognized in the pertinent art of Lee. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Lee by forming an oxide on the substrate prior to depositing the silicon nitride layer, lining the isolation trenches prior to depositing the oxide layer nor fabricating semiconductor device structures on the semiconductor substrate between the isolation trenches as taught by Hao et al. to prevent gaps in the isolation structures (col. 2, lines 1 and 2).

Referring to claim 13, Lee disclose the second silicon nitride etch stop layer of claim 8 wherein the second silicon nitride etch stop layer may have a thickness between 250 and 750 Angstroms (col. 4, lines 30-32). It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to have the thickness of the second silicon nitride etch stop layer to have a thickness between 500 and 2000 Angstroms since it has been held that "In such an

situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Hao et al. as applied to claims 1-10 and 13-25 above, and further in view of Rossman et al. (6,559,026).

Lee discloses a method of forming shallow trench isolation regions where a silicon nitride etch stop layer (34) in deposited using a chemical vapor process (CVD) on to a semiconductor substrate (30); etching a plurality of isolation trenches (Fig. 6) through the silicon nitride etch stop layer (34) into the semiconductor substrate (30), whereby narrow active areas and wide active areas of the semiconductor substrate (30) are left between the isolation trenches; depositing an oxide layer (38) over the silicon nitride etch stop layer (34) and within the isolation trenches using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (38) overlying the silicon nitride etch stop layer (34) and then removing the silicon nitride etch stop layer (34). Lee further discloses the silicon nitride etch stop layer (34) having a thickness between 1500 and 2500 Angstroms, and the removing the silicon nitride etch stop layer (34) with a hot phosphoric acid (H_3PO_4) dip (col. 3, lines 38-65; col. 4, lines 59-65). Lee also discloses depositing a second silicon nitride etch stop layer (46), with a thickness between 250 and 750 Angstroms, over the oxide layer (38), removing the second silicon nitride etch stop layer (38) overlying the wide active areas, etching away the oxide layer

(38) overlying the silicon nitride etch stop layer (34) and the removing the silicon nitride etch stop layer (34) and the second silicon nitride etch stop layer (46) (col. 4, lines 33-65).

Lee in view of Hao et al. do not disclose the HDP-CVD having a sputtering ratio of 3.5 during the deposition of the oxide layer and a sputtering ratio of 2 during the deposition of the second silicon nitride etch stop layer.

Rossman et al. disclose a method of forming shallow trench isolation regions where a silicon nitride etch stop layer (13) is formed on a semiconductor substrate (12), etching through the silicon nitride etch stop layer (13) into the semiconductor substrate (12) to form isolation trenches (14), whereby narrow active areas and wide active areas of the semiconductor substrate (30) are left between the isolation trenches (14) and forming an oxide layer (26) over the silicon nitride layer and in the isolation trench using a HDP-CVD process (col. 1,lines 27-47). Rossman et al. further disclose the HDP-CVD having a sputtering ratio of 3.5 (col. 17, lines 43-47).

Since Lee and Rossman et al. are both from the same field of endeavor, a method of forming shallow trench isolation regions where, the purpose disclosed by Rossman et al. would have been recognized in the pertinent art of Lee. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Lee by the HDP-CVD having a sputtering ratio of 3.5 as taught by Rossman et al. to prevent voids in the filling on the isolation trenches (col. 2, line 66, col. 17, lines 43-47).

Referring to claim 12, Rossman et al. do not disclose a sputtering ratio of 2. It would have been obvious to one having ordinary skill in the art at the time invention was made to have a sputtering ratio of 2 as disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fu et al. (6,426,272) disclose a method of forming shallow trench isolation regions where the trench fill is formed using an HDP-CVD process with a deposition component and a sputtering component.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (703) 605-4299. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

pep
May 7, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800